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10/783,195	02/20/2004	Mou-Shiung Lin	MS98-002CCC CIPB	6169

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,195	LIN ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *106-110,112-116,119,120,123,126-129,131 and 136-155* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *106-110,112-116,119,120,123,126-129,131 and 136-155* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 120, 123, 126-129, 136, 139-140, 143-153, and155 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Reciting a newly added limitation "a circuit interconnection wirebonded to said metal" in claim 120,136, and 152 is lacking of support in the originally disclosed specification. Claims 123, 126-129, 139-140, 143-153 and 155 are rejected for virtually depending on rejected claims 120 and 136.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 106, 107-109, 110, 112, 113, 116, 119, 136, 141-142, and 151 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6605549 to Leu et al. of record

Regarding claim 106, Leu disclòses in fig. 4E a semiconductor chip or wafer comprising: a silicon substrate 40; a metallization structure 47 over said silicon substrate 40, a passivation layer 55 over said first-metallization structure 47, wherein an opening in said passivation layer exposes said first contact pad 47 of said metallization structure, and wherein said passivation layer comprises an inorganic material, col. 7 line 20; a polymer layer 42, col. 8 line10, over said passivation layer 55, wherein said polymer layer has a thickness of between 0.05- 5 micron, col. 8 line 23, and a metal trace 53 over part of said polymer layer 42 and over said first contact pad 47, wherein said metal trace 53 comprises a gold layer, col. 10 line 24, with a thickness of between 2 and 100 micron (fig. 4e shows the gold layer 52 is at least equal or thicker than the dielectric layer 42), and wherein said metal trace comprises a second contact pad (where 49A is located) connected to said first contact pad 47, and wherein the positions of said first and second contact pads from a top view are different, fig. 4E.

Regarding claims 107-109, Leu discloses the semiconductor chip wherein passivation 55 comprises a topmost nitride or oxide layer of said semiconductor chip or wafer, col. 7 lines 19-25.

With respect to "wherein said passivation layer comprises a topmost CVD-formed layer" is considered to be a process that does not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claims 110 and 112, Leu discloses the semiconductor device where the metal trace 53 further comprises a titanium-containing layer 45 under the gold layer 53.

With respect to "second pad is used to be wirebonded thereto", the structure recited in Leu is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claims 113 and 119, Leu discloses the semiconductor chip or wafer wherein the metal trace comprises gold.

The process limitations "electroplated" and wirebond in claims 129 and 131 do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claims 116, 151, Leu discloses the semiconductor chip or wafer wherein no polymer layer is over the metal trace 53, fig. 4E.

Regarding claim 141-142, Leu discloses the semiconductor chip or wafer wherein said titanium-containing layer 45 has a thickness of between 0.005 and 0.1

micron, col. 9 line 20, wherein said metal trace further comprises another gold layer 50 between said titanium-containing layer 45 and said gold layer 52, wherein said another gold layer 50 has a thickness of between 0.1 and 0.3 micron, col. 9 line 43.

Regarding claims 136, Leu discloses a circuit circuitry component comprising: a semiconductor substrate 40; a metallization structure 47 over said semiconductor substrate 40; a passivation layer 55 over said metallization structure 47, wherein said passivation layer comprises an inorganic material; and a metal trace 53 over said passivation layer 55, wherein said metal trace 53 comprises a titanium-containing laver 45, a first gold layer 50 on said titanium-containing laver 45, and a second gold layer 53 on said first gold layer 50, wherein said titanium-containing laver has a thickness of about 0.005-0.1 micron said first gold laver has a thickness of between 0.1-0.3 micron, col. 9 line 20 and 43 and a said second gold layer 53 a thickness of about 5 micron ((fig. 4e shows the gold layer 52 is at least equal or thicker than the dielectric layer 42 that has a thickness of about 0.05 to 5 micron), see discussion in claim 106 above.

Regarding claim 154, Kikuchi discloses the circuit component wherein said polymer layer 140 comprises polyimide [0040].

5. Claims 120, 123, 126-129, 131, and 136-140, 143-145, 148-150, 152, and 154-155 are rejected under 35 U.S.C. 102(e) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over US 2003/0102551 to Kikuchi of record.

Regarding claim 120, Kikuchi discloses a semiconductor chip or wafer in fig. 2 comprising: a silicon substrate 110 [0030] (semiconductor comprises silicon), metallization structure 120 [0038], over said silicon substrate 110; a passivation layer

130 [0039] over said metallization structure 120; wherein an opening in said passivation layer 130 exposes a first contact pad of metallization structure 120, and wherein said passivation layer 130 comprises an inorganic material [0039]; and a metal trace 160 [0043], over part of said passivation layer 130 and over said first contact pad 120, fig. 2, wherein said metal trace 160 comprises a gold layer with a thickness of between 2 and 100 μm [0043], wherein said metal trace 160 comprises a second pad (where 170 is located), fig. 2, connected to said first pad, wherein the positions of said first and second contact pads from a top view are different, fig. 1, a circuit interconnect 170/190 wirebonded to said second contact pad [0046].

With respect to "wirebonded to" is considered process limitations that do not carry weight in a claim drawn to structure. In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985), MPEP 2113.

Regarding claims 123, 129, 131, and 140, Kikuchi discloses the semiconductor chip or wafer further comprising a polymer layer 140 over said passivation layer 130, wherein said second contact pad is over said polymer layer, fig. 2, wherein the metal trace comprises gold.

The process limitations "electroplated" and wirebond in claims 129 and 131 do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claims126-128, 148-150, Kikuchi discloses the semiconductor chip wherein passivation 130 comprises a topmost nitride or oxide layer of said semiconductor chip or wafer [0039]

With respect to "wherein said passivation layer comprises a topmost CVD-formed layer" and "electroplated" is considered to be a process that does not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

With respect to "second contact pad is used to be wirebonded thereto" does not provide a structural limitation, but it is rather defining the second pad is capable of having or receiving a wirebonded thereto. Thus, the second pad of Kikuchi would have the same capability as claimed. Furthermore, the structure recited in Kikuchi is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claims 136, 152, Kikuchi discloses a circuit circuitry component comprising: a semiconductor substrate 110; a metallization structure 120 over said semiconductor substrate 110; a passivation layer 130 over said metallization structure, wherein said passivation layer comprises an inorganic material; and a metal trace 160 over said passivation layer 130, wherein said metal trace 160 comprises a titanium-containing laver, a first gold layer (layer 150) on said titanium-containing laver, and a second gold layer on said first gold layer, wherein said titanium-containing laver has a thickness of about 0.15 micron said first gold laver has a thickness of between 0.6

micron [0043) and a said second gold layer a thickness of between 5 micron [0043], a circuit interconnect 170/190 wirebonded to said second contact pad [0046].

With respect to "wirebonded to" is considered a process limitation that does not carry weight in a claim drawn to structure. In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985), MPEP 2113.

Regarding claims 137-138, Kikuchi discloses the semiconductor chip or wafer wherein said second contact pad is used to be wirebonded thereto, and further comprising a metal bump 170 or solder bump 190 [0043] and [0046] over said second pad, fig. 2.

Regarding claim 139, Kikuchi discloses the semiconductor chip or wafer wherein further comprising a polymer layer 140 [0040] between said metal trace 160 and said passivation layer 130.

Regarding claim 143-145, see discussion in claim 136.

Regarding claim 153-155, Kikuchi discloses the circuit component wherein said polymer layer 140 comprises polyimide [0040].

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 114-115 and 154 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6605549 to Leu et al. in view of US 2003/0102551 to Kikuchi

Regarding claims 114-115, Leu does not disclose the semiconductor device further comprises a metal or solder bump over the second contact.

However, Kikuchi discloses in fig. 12 disclose the semiconductor device further comprises a metal or solder bump over 190/170 the second contact. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the teaching of metal bump teaching Kikuchi with Leu'device, because such metal bump would have allowed further interconnection and improved the device reliability as taught by Kikuchi, see abstract.

Regarding claim 154, Leu does not disclose the circuit component wherein said polymer layer 42 comprises polyimide.

However, Leu discloses the dielectric layer 42 comprises low k-polymeric, organic and other, col. 8 lines 9-15. At the time the invention was made; it would have been obvious to a person having ordinary skill in the art to replace the dielectric 42 teaching of Leu with polyimide dielectric layer, because such polyimide dielectric material is well know in art as a inter dielectric layer, see layer 140 of Kikuchi in [0040].

9. Claims 146-147 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 2003/0102551 to Kikuchi in view of US 6605549 to Leu et al.

Regarding claim 146-147, Kikuchi does not disclose the polymer layer 140 has a thickness of about 2 and 50 micron.

However, Kikuchi discloses the polymer layer 140 has a thickness of about 1 micron [0040]. And Leu discloses a polymer layer 42 has a thickness of about 0.05 and 5 micron, col. 8 line 22. Accordingly, it would have been obvious to one of ordinary skill in art to use the thickness teaching of Leu with Kikuchi's device in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Response to Arguments

10. Applicant argues that the left metal layer 52 in the trenches 49A-B of Leu is dramatically smaller than that of the layer 42. The Examiner respectfully disagrees

because the metal material filled the trenches 49B; thus the final thickness of metal layer 52 after CMP is still at least equal to that of the layer 42 as depicted as 54 in fig. 4E.

11. Applicant argues Kikuchi fails to disclose a interconnecting structure wirebonded to said second contact pad. The Examiner respectfully disagree because Kikuchi clearly discloses the external terminal190 and interconnect 170 can be used to mount the substrate 110 on a circuit board [0046]. With respect to "wirebonded to" is considered a process limitation that does not carry weight in a claim drawn to structure. In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985), MPEP 2113.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

13 July 2007

THAO X. LE
PRIMARY PATENT EXAMINER